

In the Specification

The specification has been amended as follows:

Amend the paragraph beginning at page 8 as follows:

Importantly, the center bus chips are stacked with an offset in a single direction. The top layer of chips is wire bonded to the opposite side of the module substrate. The center bus is made to traverse to the substrate between two devices on the lower layer. To assemble the offset stacking devices into a high density module, devices are placed sequentially on a module substrate such that approximately one half of the protruding lower memory device is used as a support for the overhanging upper memory device chip of the next device stack. Fig. ~~2A-2~~ is a partial schematic of a double density stack assembly of the present invention. A dual in-line memory module (DIMM) substrate 200 supports multiple layers of device memory chips. A discrete device or spacer 202 begins the lower layer assembly having connections to the substrate via ball grid arrays 204, or the like. An offset stacked DRAM is next place such that the offset half of the upper device in the stack rests on the initial discrete device or spacer 202 for support. Subsequent offset stacked devices are then placed, each upper device 208 resting on the lower of the stack previously placed for support, fully populating the module. The exposed half of the lower chip in the final offset stack place remains uncovered.